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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,573	06/29/2001	Yoshio Hagihara	15162/03810	7850

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EXAMINER
GLASS, CHRISTOPHER W

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 03/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,573	HAGIHARA, YOSHIO	
	Examiner	Art Unit	
	Christopher W. Glass	2878	

-- The MAILING DATE of this communication appears on th c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments concerning claims 1-8 and 10-15, filed December 17, 2002, have been fully considered but they are not persuasive. Applicant argues on pages 12 and 13 that the rejection of claims 1-8 and 10-15 under 35 U.S.C. § 103(a) are improper, and contends that "absent the benefit of improper hindsight there is no motivation for one skilled in the art to modify the Shinotsuka device" (U.S. Patent No. 6,191,408 to Shinotsuka et al.) with the teachings of Dhuse (U.S. Patent No. 6,133,862 to Dhuse et al.). Applicant argues that "the reference pixels (of Dhuse) do not compensate for variations among various properties of the pixels" and holds that these pixels "are used for a different purpose altogether" (third paragraph of page 12 and first paragraph of page 13, respectively). The examiner respectfully disagrees with these arguments. The Shinotsuka reference specifically teaches compensation for variations of the various properties of the pixels, through the use of correction circuitry "for the correction of individual output values of the photosensors" by which "a fixed pattern noise resulting from the pixel-to-pixel output characteristic variation can be suppressed" (Column 2, lines 28-29 and 36-39). Regarding the subject matter of claims 1 and 15, as stated in the previous office action, Shinotsuka discloses all limitations recited, with the exception of specifically teaching the compensation means being in pixel form within the image sensing device. The teaching of Dhuse was incorporated to show that pixel-form compensation means are well known in the art. Further, the examiner disagrees that the pixels of Dhuse are used for an altogether different purpose than to "compensate for variations among various properties of the pixels" (page 12); Dhuse states that these elements are used "to eliminate the noise which is generated by the reset

of the photodiode" and specifically teaches correcting the output signals of active pixels (Column 2, lines 20-22, see also Column 7, lines 20-35). It is therefore maintained that this rejection is proper. All pending claims are considered unpatentable, according to the following rejections; while the rejection of claim 9 under 35 U.S.C. § 112 is withdrawn, a rejection on the merits of this claim appears below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,191,408 to Shinotsuka et al (Shinotsuka), in view of U.S. Patent No. 6,133,862 to Dhuse et al (Dhuse).

Regarding claims 1-3,13, and 16: Shinotsuka shows in Figure 1 a solid-state image-sensing device comprising a plurality of pixels **4** including a photoelectric conversion element and capable of generating an output signal that is logarithmically proportional to an amount of light incident on the photoelectric conversion element. Also disclosed in Figure 4 is correction circuitry **6** which operates to provide a compensation signal for compensating the output signal of the pixels, reducing signal noise that is caused by the first pixel (see Column 2, lines 25-39), as well as reading circuits **2,3** for reading out the output signals of the first and second pixels (see Column 4, lines 31-40). Shinotsuka does not specifically teach the compensation circuitry as provided in the form of second pixels disposed in the main array. However, it is well known in

solid-state image-sensing devices having a plurality of pixels to designate first pixels for generating an output signal and a plurality of second pixels for generating a signal to be used to compensate for unwanted aspects of the first pixel signals. Figure 5 of Dhuse shows a solid-state image-sensing device which comprises first pixels **502A-502N,506A-506N,510A-510N** for generating an output signal, and second pixels **400,516,518** used as reference pixels for deriving an adjustment value to compensate for unwanted noise aspects obtained in the first pixel signals (see Column 6, lines 65-67 and Column 7, lines 1-9 and 21-36). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the correction circuitry **6** of Shinotsuka in the form of a pixel, and to dispose this second pixel in the array of original pixels **4**, in order to consolidate the compensation and output signal elements rather than separating them, which would require more space. Also, by designating separate, second pixels to obtain a correction signal value, the correction signals applied to the first pixels would not be biased by problems inherent to the first output signal pixels.

Regarding claim 4: The modified solid-state image-sensing device of Shinotsuka teaches the first pixels (e.g. **4**, Shinotsuka, Figure 1) as arranged in a two-dimensional array, and the second pixels (e.g. reference pixels **400,516,518**, Figure 5, Dhuse) arranged in a line in such a way to correspond one-to-one to *rows* of the first pixels. This configuration does not expressly disclose the second pixels as provided in a line in such a way as to correspond one-to-one to *columns* of the first pixels. However, this would only involve rearrangement of these components, and it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

Regarding claim 5: The modified device of Shinotsuka comprises output signal lines provided, one for each column, permitting the output signals of the first and second pixels arranged in an identical column to be extracted therethrough (see column driver circuit **3**, Figure 1, and Column 4, lines 37-40).

Regarding claim 6: The modified device of Shinotsuka does not expressly disclose the second pixels as being smaller in size than the first pixels, but it would have been obvious to one having ordinary skill in the time the invention was made to configure them in this manner, in order to minimize the space taken by the compensation pixels and allow the maximum area for obtaining signals to be provided to the first, signal-generating pixels. Also, a change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

Regarding claim 7: The first and second pixels in the modified device of Shinotsuka inherently have different circuit configurations, since one pixel performs signal output and one performs compensation.

Regarding claim 8: As disclosed in Shinotsuka, the first pixels **4** of the modified device include a photoelectric conversion element **PD** (see Figure 2), and the second pixels, corresponding to the correction device **6** of Figures 4 and 5, include no photoelectric conversion elements.

Regarding claim 9: The modified device of Shinotsuka does not specifically teach the first and second pixels, corresponding to the pixel having the photoelectric conversion element and the pixel generating the compensation signal, as having an identical circuit configuration. However, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to arrange both types of pixels, or all pixels in the image-sensing device, to have identical circuitry (therefore each comprising photoelectric conversion components and also compensation means), in order to provide the ability to selectively designate certain pixels of the array as compensation pixels and certain pixels as active illumination-sensitive pixels, rather than being limited to an arrangement of permanently fixed roles in corresponding sections of the array.

Regarding claim 10: The modified device of Shinotsuka does not specifically teach the first and second pixels as receiving different voltages (see pixel-cell architecture of Shinotsuka, Figure 1, and Dhuse, Figures 2 and 4). However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have configured the device to provide separate voltages to the first and second pixels. This arrangement would prevent voltage fluctuations or errors in either the signal-outputting or compensating pixels from affecting the other respective pixel and therefore the compensation adjustments.

Regarding claim 11: The first and second pixels of the modified device of Shinotsuka each include a plurality of MOS transistors **Q1,Q2,Q3** included in the pixel cell architecture (see Figure 2).

Regarding claims 12 and 15: As shown in Figure 3 of Shinotsuka, the output voltage of the pixel **4** remains linear until point **Y**, at which a higher illumination level is sufficient to produce a change to logarithmic output voltage behavior. The modified device of Shinotsuka can therefore selectively generate either a linear or logarithmic output signal, depending upon the illumination provided to the photodiode (e.g. **PD**, Figure 2). It would have been obvious to also include in the modified device an optical shutter or filter which is selectively placeable over the

photodiode **PD** of the pixels, in order to regulate the amount of light entering this device and therefore the output voltage generated for controlling the type of output (linear or logarithmic) produced.

Regarding claim 14: The modified device of Shinotsuka shows in Figures 4 and 5 the compensation circuitry **6** as including a storage circuit **7** for storing the output signal of the second pixel (signal for compensation). It also shows a data comparator **8** for comparing the first pixel signal with correction data values (see Column 7, lines 9-18). It does not specifically teach the use of a differential amplifier circuit for outputting a difference between the output signal of the first pixel and the output signal of the second pixel stored in the storage circuit. However, the setup shown by Figures 4 and 5 of Shinotsuka is functionally equivalent in terms of analyzing a signal obtained by first pixels with compensation values, and it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement a differential amplifier for this purpose, in order to compare compensation and signal data and provide an amplified signal for adjustment and read-out purposes.

Regarding claim 17: Figure 16 of Shinotshuka shows the device as comprising a memory (storage devices **21,22** within section **20**) for storing the second pixel output signal, as well as for storing compensation data (see Column 8, line 18 - Column 9, line 39).

Regarding claims 18-20: Although Shinotsuka discloses that the signal noise caused by the first pixel is associated with the output signal of the pixel, it does not specifically teach this noise as being the result of a switching action of a semiconductor device in the system, or more specifically, the result of a transistor being turned off or the first pixel being reset. However, it is well known in the art to compensate for noise created by such actions or components, as taught

by Dhuse. The reference/compensation pixels in Dhuse are used "to eliminate the noise which is generated by the reset of the photodiode" signals of active pixels (Column 2, lines 20-22, see also Column 7, lines 20-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to compensate through such means for the noise created by the reset of a pixel in Shinotsuka, or the activation or deactivation of a transistor or any other device in the system, in order to counter any unwanted noise created by the operation and output of active pixels.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher W. Glass whose telephone number is 703-305-1980. The examiner can normally be reached 9:30am-6:00pm, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached at 703-308-4852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

cg
February 24, 2003

STEPHONE ALLEN
PRIMARY EXAMINER